REMARKS

This communication is in response to the Office Action of July 30, 2004. The Examiner rejected claims 25-44. Claims 25, 30, 33, 34, 37, 38, 41, and 43 were amended. Claims 25-44 are pending.

Independent claims 25, 30, 37, and 41 were amended to clarify that the bus is an I/O bus, that the graphics module is a graphics accelerator, and that the number of data transfers across the I/O bus is reduced by caching vertex data in the graphics accelerator. Support for this amendment is found in Figure 1 of Applicant's specification and on page 12, lines 5-7. The dependent claims were amended to be in accordance with the changes made to the independent claims.

Applicant's claimed invention caches vertex data in a graphics accelerator that uses vertex data to render pixel data. The graphics accelerator 15 is one of the I/O devices connected to the I/O bus 13, as described on page 5, lines 18-19. Caching vertex data in the graphics accelerator provides several benefits, such as reducing the bus bandwidth required to transfer vertex data to the graphics accelerator. Additionally, since the I/O bus must be acquired to transfer data, the number of I/O bus acquisitions required to transfer vertex data to the graphics accelerator is reduced, which improves system performance.

The Examiner rejected claims 25-29 and 37-44 as being obvious over Morgan (U.S. Pat. No. 5,821,940) in view of Rentschler (U.S. Pat. No. 5,812,950). Claims 30-36 were rejected as being obvious over Morgan in view of Rentschler and Holt (U.S. Pat. No. 5,760,792). Claims 34-35 were rejected as being obvious over Morgan in view of Rentschler and Holt and further in view of Porterfield (U.S. Pat. No. 6,069,638). Applicant respectfully traverses the rejections.

The Examiner based his rejection upon interpreting the "system bus 31" of Morgan to not be a system bus but instead to be an internal bus. The Examiner contends that the bi-directional bus coupling the display list memory and display list controller is the system bus of Morgan. The Examiner stated that: "the bus [31] cannot be the computer's system bus. It is more like an internal bus . . ." The Examiner has cited Rentschler as teaching the element of an internal bus for coupling processors such that "it would have been obvious to one of ordinary skill in the art at the time the invention was made that the system bus 31 of Morgan can not be the claimed

system bus as proved or support by Rentschler. Therefore, at least claim 25 would have been obvious by Morgan."

Applicant notes that the Examiner has not provided a source for his definitions and that there are inconsistencies in the Examiner's definitions. Moreover, it is well accepted that words in patents are to be interpreted broadly according to their ordinary meaning in light of the specification.

Nevertheless, in the interest of addressing the Examiner's concerns, Applicant has amended the claims to describe the bus element that couples the CPU to an I/O device as an I/O bus. This usage is consistent with one convention that a system bus is the bus between the CPU and main memory whereas the I/O buses are buses to I/O devices. Support for this definition is found in Exhibit 1. Additionally, it is well known in the graphics art that in one convention a graphics card (i.e., a graphics accelerator) is considered to be a type of I/O device that is coupled to an I/O bus, as described on page 3 of Exhibit 2. Note that pages 3-4 of Exhibit 2 clarify that in more complex bus architectures that the system bus can be considered to be the front side bus that connects a CPU to a bridge while examples of I/O buses includes PCI buses and AGP buses used for graphics cards.

Applicant respectfully submits that if the above-described conventions are applied to Morgan, bus 31 provides a function analogous to that of an I/O bus.[1] Morgan is a pipelined graphics display system. However, assuming that the above-described convention for a "system bus" and I/O bus are used to interpret Morgan, then a system bus coupling CPU to memory would be the bus between CPU 12 and display list memory 14. A first internal bus connects display list controller 16 to display list memory 14. A second internal bus connects transformation processor 18 to display list controller 16. Bus 31 of Morgan connects the transformation processor to the backend processor 24 of graphics display device 20. Backend processor 24 performs many of the functions of a graphics accelerator, including performing pixel rendering for generating a graphics image on graphics display device 20, as described in column 4, lines 39-42 and column 5, lines 21-24. Consequently, backend processor 24 would be considered to be an I/O device 24 and bus 31 would be an I/O bus 31. This interpretation is

[1] Applicant notes that the bus architecture of Morgan is much simpler than the embodiment of a bus architecture described in Applicant's specification. In particular, bus 31 of Morgan connects only two components and there is no indication that bus 31 must be acquired to initiate a data transfer.

further supported in regards to Figure 5 of Morgan, which shows that bus 31 is connected to an I/O buffer 30.

Note that Morgan does not cache vertex data in backend processor 24. Consequently, the transformation buffer must send a full set of transformed world space coordinates across bus 31 to backend processor 24, as described in column 4, lines 53-55.

In regards to independent apparatus claims 25 and 30 (and comparable limitations in independent method claims 37 and 41), Morgan does not teach or suggest the element of a graphics accelerator having a cache for storing vertex data. The backend processor of Morgan, which performs the pixel rendering function of a graphics accelerator, does not have a vertex cache.

Moreover, in regards to independent claims 25, 30, 37, and 41, Morgan does not teach or suggest the claimed function of a graphics accelerator that caches vertex data received from an I/O bus to reduce the number of data transfers of vertex data across the I/O bus required to render polygons. As previously described, the backend processor of Morgan does not cache vertex data received from bus 31.

Consequently, in view of the foregoing amendments and remarks, it is respectfully submitted that all pending claims in the application are now in a condition for allowance. The Examiner is invited to contact the undersigned if there are any residual issues that can be resolved through a telephone call.

The Commissioner is hereby authorized to charge any appropriate fees to Deposit Account No 03-3117.

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